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Design of Modified Shannon Based Full Adder Cell Using PTL Logic for Low Power Applications

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***Abstract*— The proposed full adder cell for low power applications has been implemented using Shannon decomposition based technique for sum and carry operation. By using the Shannon's theorem the transistor count has decreased thereby the total chip area gets minimized; hence the power also gets reduced to a considerable amount. The designs are simulated using SPICE tool which results in 25.6% improvement in power dissipation and 20% improvement in transistor count for the Modified Shannon based full adder cell when compared with MCIT based full adder cell.**

***Keywords*— Shannon's technique, power, transistor count, area, propagation delay, PTL.**

I. INTRODUCTION

Most of the Very Large Scale IC (VLSI) applications, such as digital-signal processing and microprocessors, use arithmetic operations [2]. In addition, among these widely used operations, subtraction and multiplication are most commonly used. The full adder is the building block of these operation modules. Therefore, enhancing its performance is crucial for ameliorating the performance of overall modules [3]. Such an adder can be implemented using Shannon based decomposition technique. Among the logic styles available, pass transistor logic is found to enhance the circuit performance.

II. PASS TRANSISTOR LOGIC

In PTL logic style gate and source propagates the signal. This logic style has a great functionality that can reduce the number of transistor counts. The pass transistor logic can be designed by either using pmos or nmos, but nmos is mostly desirable. This has low internodal capacitance effects and therefore PTL enables low power and high speed digital circuits. Complementary pass transistor logic is pass transistor logic with complementary inputs and outputs.

III. SHANNON THEOREM

By using this theorem any logic expression can be divided into two terms .One with a particular variable set to 1 and multiplying it by a variable and the set the variable to 0 and multiplying by its inverse. An expression can be reduced to the fullest by continuously repeating the Shannon theorem. In a generalised way Shannon theorem can be stated as a function of many variables, f ($b_0, b_1, b_2, y, b_i, y, b_n$) can be written as the sum of two terms, say one with a particular variable a_i, set to 0, and one with it set to 1.

$$f(b_0, b_1, b_2, \ldots\ldots, b_i, \ldots\ldots y, b_n) = b_i' f(b_0, b_1, b_2, \ldots\ldots, 0, \ldots\ldots y, b_n) + b_i f(b_0, b_1, b_2, \ldots\ldots, 1, \ldots\ldots y, b_n) \quad (1)$$

Shannon's theorem is applied to the logical function using n-1 variables as control inputs and three data lines set to a logical '1'. The source inputs are then connected to the V_{DD} lines (logical '0'), which are connected to the ground. The remaining n_{th} variable is connected from the data input to the source input. The data signals flow horizontally and control signals flow vertically. Pair of transistors that cancel each other are removed. The output of Shannon's expression depends upon the pass logic '1' or logic '0'. If it has logic '0' then the connection input is given by 0 and by '1' for the connection input '1'[5].

IV. ADDER ARCHITECTURE

A. Multiplexing Control Input Technique(MCIT)

MCIT technique is developed by using Karnaugh map from the Boolean expression for the sum and carry signals derived from the standard truth table for the full adder circuit.

The Boolean expressions are:

$$C = AB + BC + CA \quad (2)$$

$$S = ABC + A'B'C + AB'C' + A'BC' \quad (3)$$

By using expressions (2) and (3), the pass transistor functions can be implemented.

When expression result=0, the pass transistor function is given by the complement of the input variable. If the expression result=1, the pass transistor function is given by the input variable. In order to implement the pass transistor function for 'n' input variables, we use n-1 control input data and only one input data. The source input acts as an input of the signal.

The formulae for ith stage are given as:

$$Ci+1 = AiBi + (Ai \oplus Bi)\, Ci \quad (4)$$

$$Si = Ai \oplus Bi \oplus Ci \quad (5)$$

The full adder pass transistor using (4) and (5) are given in Fig.1 with A, A', B and B' as the pass transistor inputs and these are the multiplexing control inputs. XOR (A, B) in Fig.2 can be obtained from the stage I (differential node). The differential node XOR (A, B) and Ci are fed through the MCIT and forms XOR circuit for sum and XNOR for its complement.To receive the logic signals from the corresponding pass transistor logic trees (differential node) [6] a duality of pass transistor logic trees and a multiple input logic gate are combined in a full adder.

A complex logic operation can be expressed using this pass transfer function, by which the number the number of stages in the pass transistor logic tree gets reduced and the operation speed gets enhanced. The output expression Ai, Bi, and Ci and its complement are obtained at the restoration node. The critical path is minimized as a result of balancing the adder circuit and the bit rate conversion and operation speed also gets enhanced.

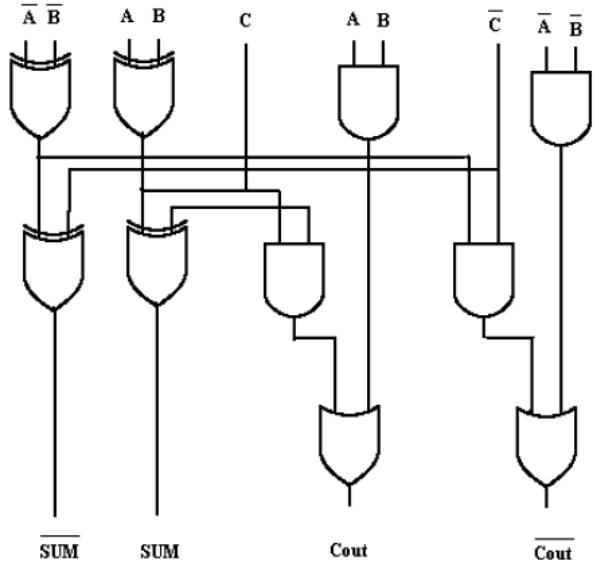

Fig. 1 MCIT for a full adder circuit using logic gates

Pass transistor logic threshold voltage loss problem is solved by just complementing the inputs and outputs and adding an inverter at the output. This approach is known as complementary pass transistor logic. Complementary pass transistor logic is pass transistor logic with complementary inputs and outputs available simultaneously. Generally, pull-up pmos transistors are necessary for swing restoration. In order to minimize the static current due to the incomplete turn-off of the nmos in the output inverter, a weak pmos feedback device is added in the CPL circuits to pull the pass transistor output to full supply voltage level. The sum circuit of this full adder cell is designed by using MCIT as shown by the broken encircled area in Fig.2.

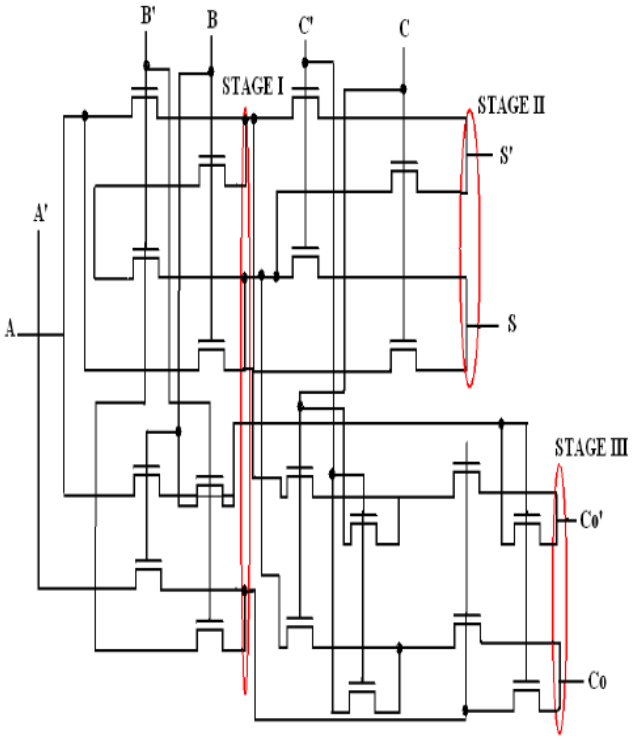

Fig. 2 MCIT for a full adder circuit using pass transistor

B. *Existing Shannon Based Full Adder Cell*

The existing full adder was designed based on "(2) and "(6)" by combining the MCIT technique for sum and Shannon operation for carry.

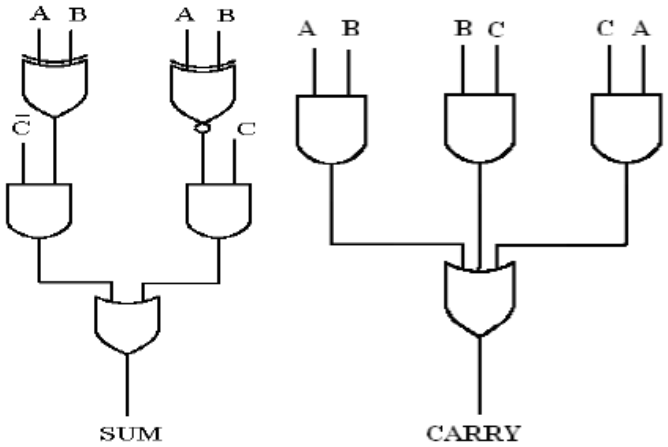

Fig. 3 Shannon based full adder using logic gates

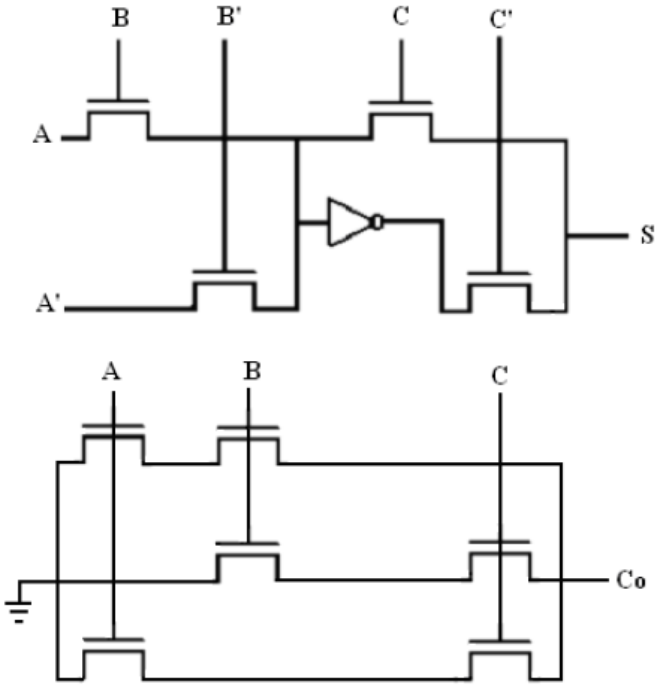

Fig. 4 Shannon based full adder using pass transistor logic

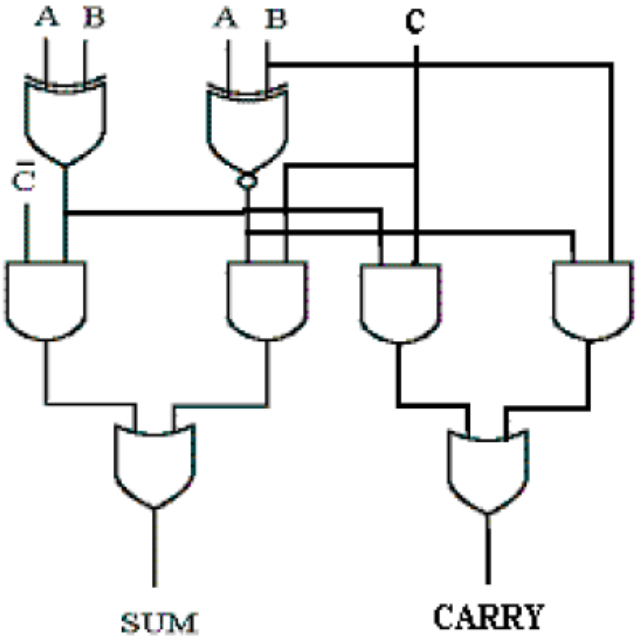

Fig. 5 Proposed Shannon based full adder using logic gates

As depicted in Fig.3 and Fig.4 inputs B and B' are used as used as the control signal of the sum circuit.

$$S = (A \oplus B)\overline{C} + \overline{(A \oplus B)}C \quad (6)$$

The equation (3) is modified as (6) and the adder is designed to reduce the transistor count to six in the sum circuit. The C and C' are the differential nodes of the circuit. Carry circuit is designed using the Shannon complementary pass transistor logic, and uses only the inputs A, B and C. It has been designed using the fundamental Shannon equation "(1)", where the source inputs are connected with logic '1', yielding an always 'ON' condition for the transistor. The actual inputs AB, BC and CA are connected in parallel to give the output C=AB+ BC+ CA. In this circuit, all the pass inputs are connected to the VDD line so that the pass gates are always 'ON' [1].

C. Proposed Shannon Based Full Adder Cell

The proposed full adders have the modified expression for the carry as:

$$C=(\overline{A \oplus B})B+(A \oplus B)C \quad (7)$$

With the Shannon's theorem the sum and carry expressions are condensed and thereby the transistor count has decreased. In the existing design of full adder the carry was generated using six transistors where as the proposed full adder design uses only two transistors. Thus the area also gets minimized and thereby power has also been reduced to considerable amount.

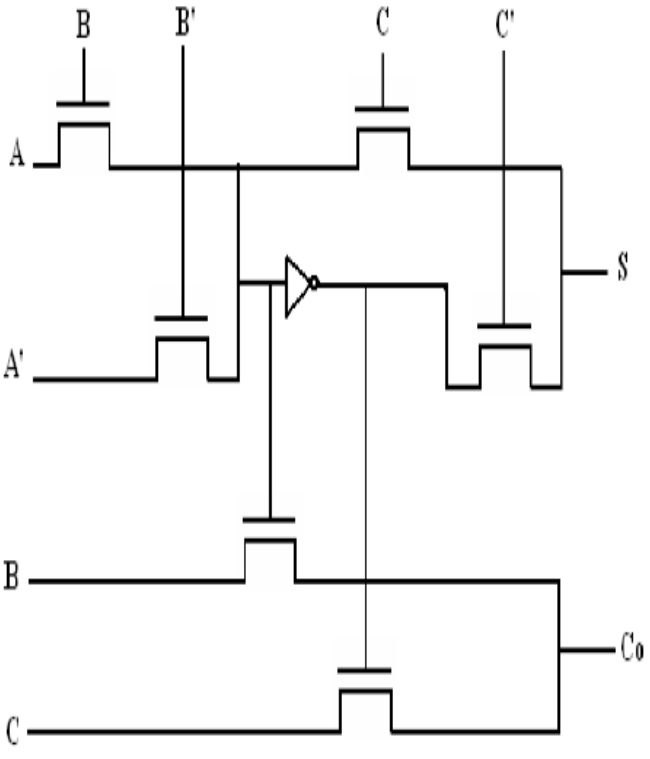

Fig. 6 Proposed Shannon based full adder using pass transistor logic

In this paper as an application we have designed a sequential 4-bit adder using the proposed full adder cell.

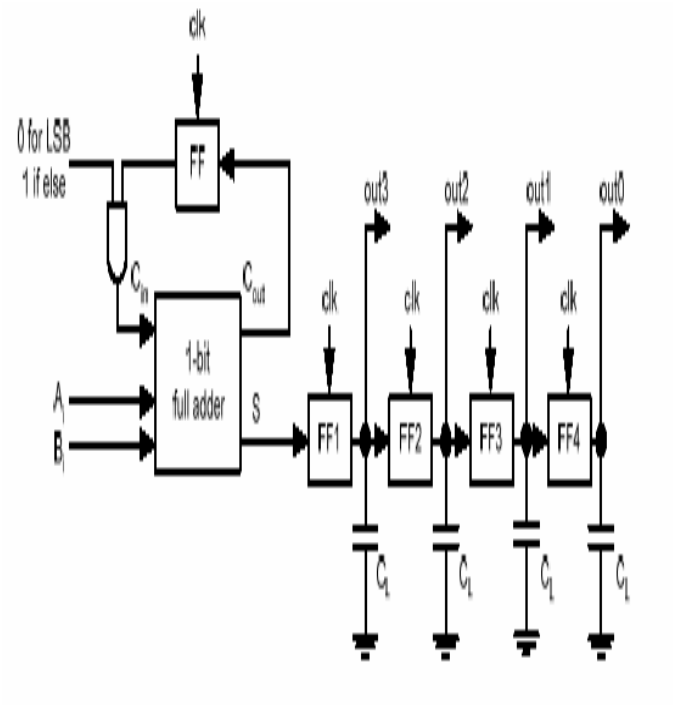

Fig. 7 Sequential 4-bit adder

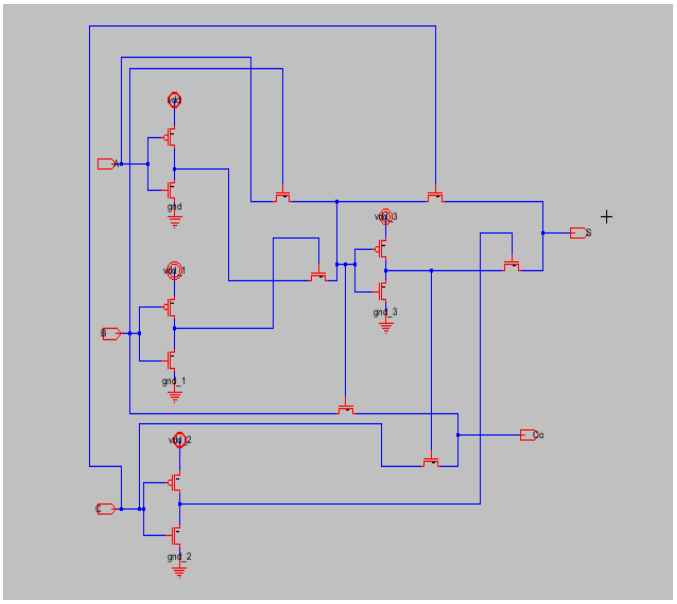

Fig. 8 Schematic of proposed modified Shannon full adder

V. Results and Discussions

From the simulation results, it was shown that the proposed modified Shannon based full adder cell using PTL logic is better than the existing method in terms of power consumption and transistor counts.

Type of full adder cell	Number of MOSFET's
MCIT based full adder cell	80
Existing Shannon	18
Proposed Modified Shannon	14

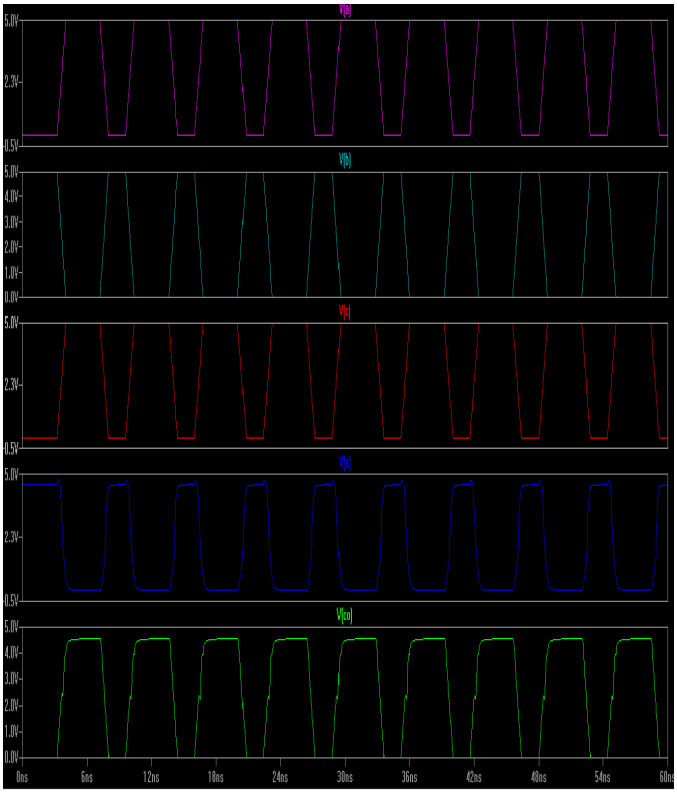

Fig. 9 Simulation results of proposed modified Shannon full adder

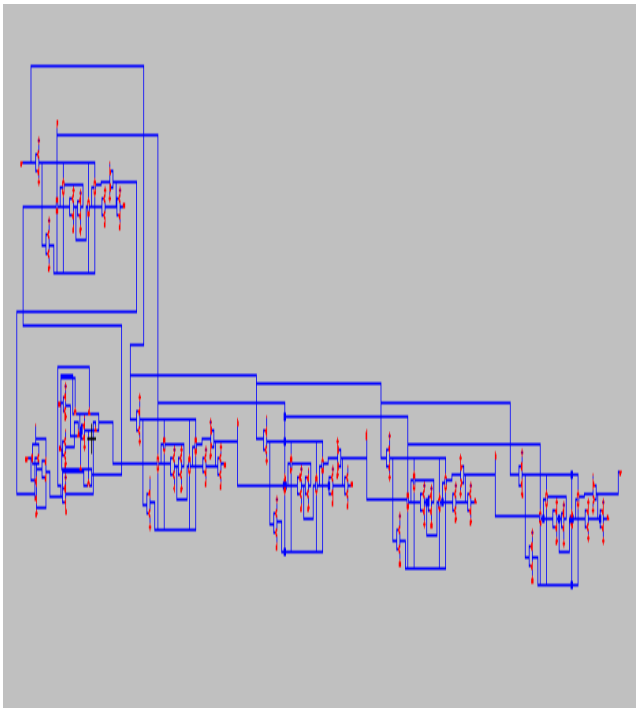

Fig. 10 Schematic of sequential 4-bit adder using the proposed full adder cell

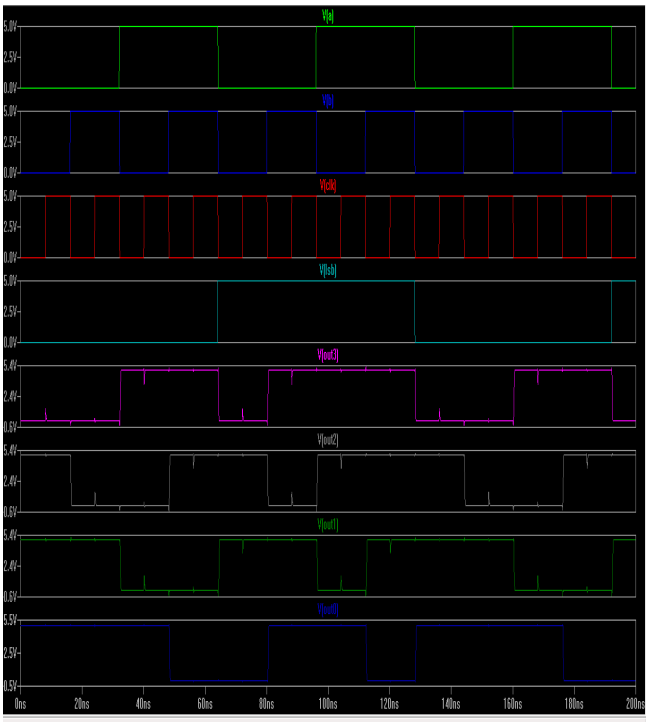

Fig. 11 Simulation results of sequential 4-bit adder using the proposed full adder cell

VI .Conclusions

The proposed modified Shannon based full adder cell has been simulated and results are compared with MCIT based full adder cell and the existing Shannon based full adder cell in terms of power, transistor count, area. This proposed adder cell is having improvement in all these aspects.

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